**Printed Page:- 04** **Subject Code:- ACSE0305-ACSEH0305**

**Roll. No:**

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**NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA**

**(An Autonomous Institute Affiliated to AKTU, Lucknow)**

**B.Tech**

**SEM: III - THEORY EXAMINATION (2023 - 2024)**

**Subject: Computer Organization & Architecture**

**Time: 3 Hours** **Max. Marks: 100**

**General Instructions:**

**IMP:** *Verify that you have received the question paper with the correct course, code, branch etc.*

***1.*** *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

***2.*** *Maximum marks for each question are indicated on right -hand side of each question.*

***3.*** *Illustrate your answers with neat sketches wherever necessary.*

***4.*** *Assume suitable data if necessary.*

***5.*** *Preferably, write the answers in sequential order.*

***6.*** *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

**SECTION-A** 20

1. Attempt all parts:-

1-a. A stack organized computer uses instruction of_____. (CO1) 1

(a) Immediate Addressing
(b) Indirect Addressing
(c) Zero addressing
(d) Two- addressing

1-b. Daisy Chain Arbitration is a type of _____ Bus arbitration.(CO1) 1

(a) Serial
(b) Parallel
(c) Dynamic
(d) All above

1-c. _____ is a representation of floating point numbers.(CO2) 1

(a) IEEE752
(b) IEEE754
(c) IEEE802
(d) None of these

1-d. The sign 2's complement representation of -9 is _____. (CO2) 1

(a) 10000
(b) 10010
(c) 10111

(d) 11011

1-e. Highly encoded schemes that use compact codes to specify a small number of functions in each micro instruction is (CO3) 1

(a) Horizontal organisation
(b) Vertical organisation
(c) Diagonal organisation
(d) None of the mentioned

1-f. A sequence of control words corresponding to a control sequence is called (CO3) 1

(a) Micro routine
(b) Micro function
(c) Micro procedure
(d) None of the mentioned

1-g. _____ memory has the fastest speed in the computer memory hierarchy (CO4) 1

(a) Cache
(b) Register
(c) RAM
(d) ROM

1-h. The circuit used to store one bit of data is known as ___ (CO4) 1

(a) RAM
(b) ROM
(c) Flip-Flop
(d) None of above

1-i. Instructions that are read from memory by an IOP are sometimes called _____, to distinguish them from instructions that are read by the CPU. (CO5) 1

(a) Commands
(b) Instructions
(c) Program
(d) Subroutine

1-j. In memory-mapped I/O (CO5) 1

(a) The I/O devices have a separate address space
(b) A part of the memory is specifically set aside for the I/O operation
(c) The I/O devices and the memory share the same address space
(d) The memory and I/O devices have an associated address space

2. Attempt all parts:-

2.a. Define Bus Arbitration. (CO1) 2

2.b. Explain Array Multiplier.(CO2) 2

2.c. Write down five steps of instruction cycle.(CO3) 2

| | | |
|---|---|---|
| 2.d. | Define tag in cache mapping.(CO4) | 2 |
| 2.e. | Why are the read and write control lines in DMA bidirectional?(CO5) | 2 |

**SECTION-B** 30

3. Answer any five of the following:-

| | | |
|---|---|---|
| 3-a. | Draw the diagram of four bit common bus system for four registers with the use of Multiplexer. Explain how it works. (CO1) | 6 |
| 3-b. | Explain sequence of microoperations for implementing PUSH and POP instructions in the register stack and memory stack. (CO1) | 6 |
| 3-c. | Explain Carry-look ahead adder with logic diagram. (CO2). | 6 |
| 3-d. | Explain single precision and double precision representation of floating point numbers with an example.(CO2) | 6 |
| 3.e. | Differentiate between hardwired and micro programmed control unit. (CO3) | 6 |
| 3.f. | Explain memory hierarchy with suitable diagram. What are the different levels in memory hierarchy? (CO4) | 6 |
| 3.g. | Explain CPU-IOP communication. Also draw the flowchart showing the sequence of operation to be carried out during communication.(CO5) | 6 |

**SECTION-C** 50

4. Answer any one of the following:-

| | | |
|---|---|---|
| 4-a. | A digital computer has a common bus system for 4 registers of 8 bits each and the bus is constructed with multiplexers.<br>a. How many multiplexers are there in the bus?<br>b. What size of multiplexers are needed?<br>c. Draw the block diagram that implements this. (CO1) | 10 |
| 4-b. | Explain seven registers CPU organization with the help of block diagram and control word. (CO1) | 10 |

5. Answer any one of the following:-

| | | |
|---|---|---|
| 5-a. | Calculate -9 X -13 with the help of Booth algorithm using flow chart. (CO2) | 10 |
| 5-b. | Sketch the array multiplier of 4 bit binary numbers, multiplicand is (b3 b2 b1 b0) & multiplier is (a2 a1 a0) with AND gates and full adders. (CO2) | 10 |

6. Answer any one of the following:-

| | | |
|---|---|---|
| 6-a. | Give the micro instruction format and specify the working of each field.(CO3) | 10 |
| 6-b. | Write program to evaluate the arithmetic statement:X = (A+B)*(C+D) using zero, one, two and three address instructions.(CO3) | 10 |

7. Answer any one of the following:-

| | | |
|---|---|---|
| 7-a. | Explain Content Addressable memory with neat diagram. (CO4) | 10 |
| 7-b. | How the mapping is done between cache and main memory? Explain at least two methods of mapping. (CO4) | 10 |

8. Answer any one of the following:-

| | | |
|---|---|---|
| 8-a. | Perform LRU and FIFO page replacement algorithm for frame size 3 which is | 10 |

empty in starting and reference string is 7,1,2,3,4,3,5,7,4,5.Find out page fault and hit ratio.(CO5)

8-b. What is DMA Controller? Draw and explain the block diagram of DMA Controller. (CO5) 10